ESP-S3-12K Specification

Version V1.0.0

Document resume

Version	Date	Develop/revise content	Edition	Approve
V1.0.0	2021.11.22	First Edition	ChaoMeiDeng	NingGuan

Content

1. Product Overview

ESP-S3-12 is a Wi-Fi+BLE module developed by Shenzhen Ai-Thinker Technology Co., LTD.The core processor chip ESP32-S3 is a highly integrated, low-power Wi-Fi and Bluetooth system-on-chip (SoC),designed for Internet of Things (IoT), mobile devices, wearable electronics, smart home and other applications.

ESP32-S3 chips offer industry-leading low power performance and rf performance,Support WiFi IEEE802.11b/ G/N protocol and Bluetooth 5.The chip is powered by xTENSA-R 32-bit LX7 dual-core processor and operates at up to 240 MHz. Support secondary development without the use of other microcontrollers or processors.Chip built-in 512 KB SRAM, 384 KB ROM, 16KB RTC SRAM. The chip supports a variety of low-power working states and can meet the power requirements of various application scenarios.The precise clock gating function, dynamic voltage clock frequency regulation function and rf output power adjustment function of the chip can achieve the best balance between communication distance, communication rate and power consumption.

ESP-S3-12K module provides a variety of peripheral interfaces, including UART, PWM, SPI, I2S, I2C, ADC, LCD, DVP,RMT(TX/RX), pulse counter,USB OTG，USB Serial/JTAG，SDIO，DMA controller, TWAI controller, temperature sensor, capacitive sensor and up to 38 IO ports.

ESP-S3-12K module has a variety of unique hardware security mechanisms. Hardware encryption accelerator supports AES, SHA and RSA algorithms.The RNG, HMAC and Digital Signature modules provide more security features. Other security features include Flash encryption and secure boot signature verification. The perfect security mechanism enables the chip to be perfectly applied to various encryption products.

ESP-S3-12K module supports low power Bluetooth: Bluetooth5, Bluetooth Mesh. Bluetooth speed support: 125Kbps, 500Kbps, 1Mbps, 2Mbps. Support broadcast extension, multi - broadcast, channel selection.

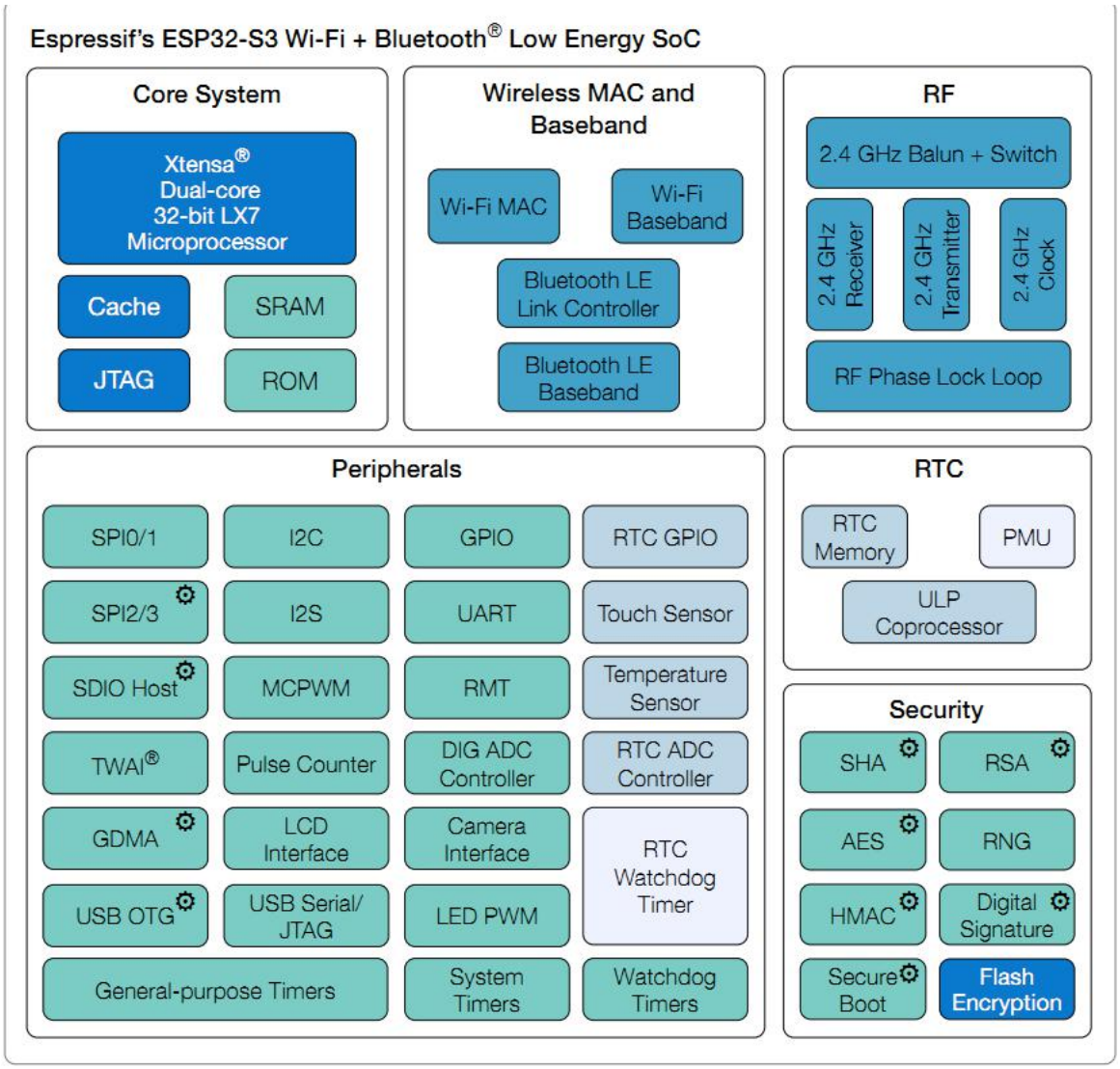


Figure 1 Main chip architecture diagram

1.1. Characteristic

- Support WiFi 802.11b/g/ N, 1T1R mode data rate up to 150Mbps
- Support Bluetooth5, Bluetooth Mesh, speed support: 125Kbps, 500Kbps, 1Mbps, 2Mbps
- Xtensa-R32-bit LX7 dual-core processor, supports clock frequency up to 240 MHz, has 512 KB SRAM, 384 KB ROM, and 16KB RTC SRAM
- Support UART/GPIO/ADC/PWM/I2C/I2S/SPI/LCD/DVP/RMT/SDIO/USB OTG USB Serial/MCPWM/DMA controller/TWAI controller interface, temperature sensor, pulse counter, capacitive sensors GPIO

- The package is SMD-42
- Integration WiFi MAC/BB/RF/PA/LNA/Bluebooth
- Multiple sleep modes are supported and the deep sleep current is less than 8uA
- The serial port rate is up to 5Mbps
- Supports STA/AP/STA+AP and hybrid modes
- Smart Config (APP) /AirKiss (wechat) is supported
- Support serial port local upgrade and remote firmware upgrade (FOTA)
- Fixed universal AT instruction for quick use
- Support secondary development, integrated Windows, Linux development environment
- About Flash: the esp-s3-12k module has 8MByte Flash built-in by default

2. Main parameters

Table 1 Description of the main parameters

Model	ESP-S3-12K
Package	SMD-42
Size	31*18*3.2(±0.2)mm
Antenna	Onboard antenna or IPEX external antenna
Frequency	2400 ~ 2483.5MHz
Operating temperature	-40 ℃ ~ 85 ℃
Storage temperature	-40 ℃ ~ 125 ℃ , < 90%RH
Power supply	Support voltage 3.0V ~ 3.6V，supply current >500mA
Interface	UART/GPIO/ADC/PWM/I2C/I2S/SPI/LCD/DVP/RMT/SDIO/USB OTG/MCPWM/DMA/TWAI
IO	38
UART rate	Support 110 ~ 4608000 bps ，default 115200 bps
Bluetooth	Bluetooth5，Bluetooth mesh
Security	WEP/WPA-PSK/WPA2-PSK
SPI Flash	8MByte（default）Optional 4/16MByte
PSRAM	8MByte（default）Optional 0/2MByte

2.1. Static electricity requirements

ESP-S3-12 module is an electrostatic sensitive device. Therefore, you need to take special precautions when carrying it.

Figure 2 ESD preventive measures

2.2. Electrical characteristics

Table 2 Electrical characteristics table

Parameters		Conditi	Min.	Typical value	Max.	Unit
Support voltagae		VDD	3.0	3.3	3.6	V
I/O	V_{IL}/V_{IH}	-	-0.3/0.75VDD	-	0.25VDD/VDD+0.3	V
	V_{OL}/V_{OH}	-	N/0.8VIO	-	0.1VIO/N	V
	I_{MAX}	-	-	-	40	mA

2.3. WiFi Rf Performance

Table 3 WiFi RF performance Table

Description	Typical value			Unit
Working Central Frequency	2412 - 2484			MHz
Output Power				
Rate model	**Min.**	**Typical value**	**Max.**	**Unit**
11n Model HT40，PA Output power	13	15	17	dBm
11nModel HT20，PA Output power	13	15	17	dBm
11g Model ，PA Output power	14	16	18	dBm
11b Model ，PA Output power	16	18	20	dBm
Receive Sensitivity				
Rate model	**Min.**	**Typical value**	**Max.**	**Unit**
11b，1 Mbps	-	-96	-	dBm
11b，11 Mbps	-	-88	-	dBm
11g, 6 Mbps	-	-92	-	dBm
11g，54 Mbps	-	-75	-	dBm
11n，HT20 (MCS7)	-	-73	-	dBm
11n，HT40 (MCS7)	-	-70	-	dBm

2.4. BLE Rf performance

Table 4 BLE RF performance table

Description	Typical value			Unit
Working Central Frequency	2402 - 2480			MHz
Output Power				
Rate model	**Min.**	**Typical**	**Max.**	**Unit**
1Mbps	-25	0	19	dBm
2Mbps	-25	0	19	dBm
Receive Sensitivity				
Rate model	**Min.**	**Typical**	**Max.**	**Unit**
1Mbps sensitivity @30.8%PER	-	-94	-	dBm
2Mbps sensitivity @30.8%PER	-	-90	-	dBm

2.5. Power

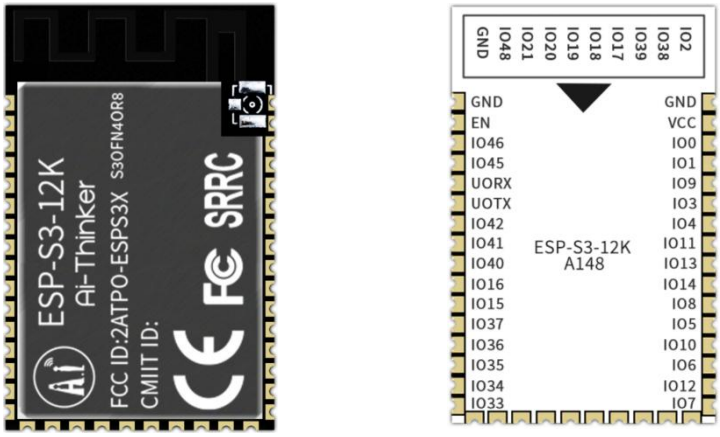
The following power consumption figures are based on a 3.3V power supply, an ambient temperature of 25°C, and an internal voltage regulator.

- All measurements were made at the antenna interface without SAW filter.
- All launch data are measured in a sustained launch mode based on a 100% duty cycle.

Table 5 Power consumption table

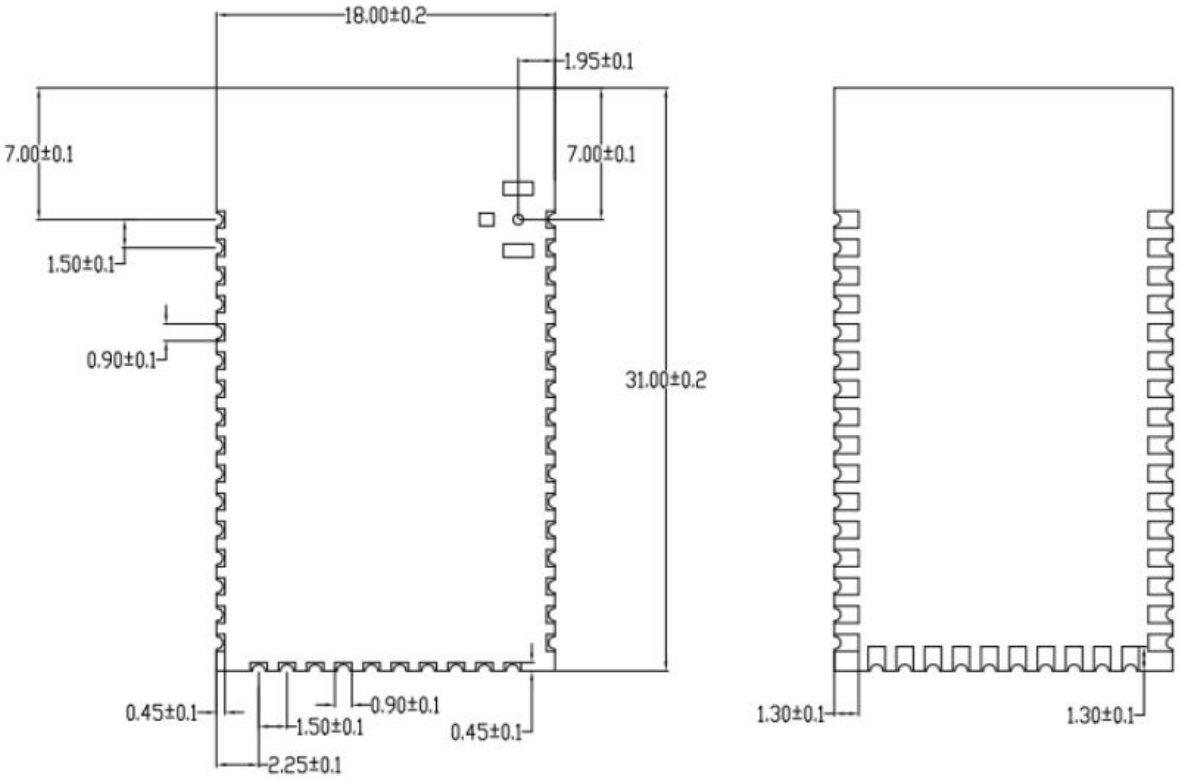
Model	Min.	AVG	Max.	Unit
Transfer 802.11b, DSSS 1Mbps, POUT=+20dBm	-	350	-	mA
Transfer 802.11g, OFDM 54Mbps, POUT =+18dBm	-	290	-	mA
Transfer 802.11n, MCS7, POUT =+17dBm	-	280	-	mA
Receive 802.11b,packet length is 1024 bytes	-	97	-	mA
Receive 802.11g,packet length is 1024 bytes	-	97	-	mA
Receive 802.11n,packet length is 1024 bytes	-	100	-	mA
Modem-Sleep①	-	20	-	mA
Light-Sleep②	-	240	-	μA
Deep-Sleep③	-	8	-	μA
Power Off	-	1	-	μA

3. Appearance dimensions



Front Back

Figure 3 Appearance diagram pictures is for reference only,subject to physical objects)



Front Back

Figure 4 Module size diagram

4. Pin definition

ESP-S3-12K module is connected with a total of 42 pins, as shown in the schematic diagram of pins, pin function definition table is the interface definition.

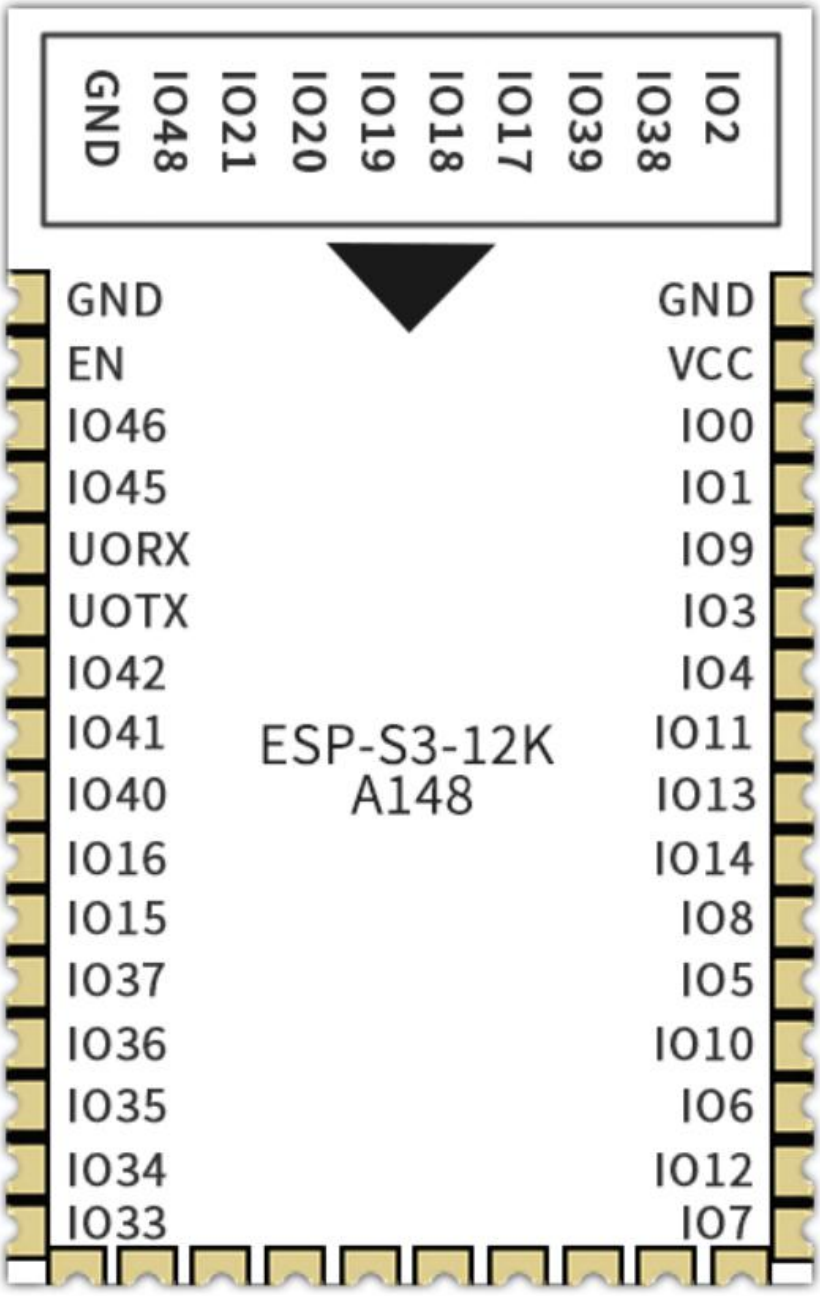


Figure 5 Schematic diagram of module pins(top view)

Table 6 Pin function definition table

No.	Name	Function
1，26，42	GND	Ground(Power negative electrode)
2	VCC	Power supply positive electrode
3	IO0	GPIO0，RTC_GPIO0
4	IO1	GPIO1,RTC_GPIO1,TOUCH1,ADC1_CH0
5	IO9	GPIO9,RTC_GPIO9,TOUCH9,ADC1_CH8, SUBSPIHD,FSPIHD
6	IO3	GPIO3,RTC_GPIO3,TOUCH3,ADC1_CH2
7	IO4	RTC_GPIO4,GPIO4,TOUCH4,ADC_CH3
8	IO11	RTC_GPIO11,GPIO11,TOUCH11,ADC2_CH0, FSPIIO5,SUBSPID,FSPID
9	IO13	RTC_GPIO13,GPIO13,TOUCH13,ADC2_CH2, FSPIIO7,SUBSPIQ,FSPIQ
10	IO14	RTC_GPIO14,GPIO14,TOUCH14,ADC2_CH3, FSPIDQS,SUBSPIWP,FSPIWP
11	IO8	RTC_GPIO8,GPIO8,TOUCH8,ADC1_CH7, SUBSPICS1
12	IO5	RTC_GPIO5,GPIO5,TOUCH5,ADC1_CH4
13	IO10	RTC_GPIO10,GPIO10,TOUCH10,ADC1_CH9, FSPIIO4,SUBSPICS0,FSPICS0
14	IO6	RTC_GPIO6,GPIO6,TOUCH6,ADC1_CH5
15	IO12	RTC_GPIO12,GPIO12,TOUCH12,ADC2_CH1, FSPIIO6,SUBSPICLK,FSPICLK
16	IO7	RTC_GPIO7,GPIO7,TOUCH7,ADC1_CH6
17	IO2	RTC_GPIO2,GPIO2,TOUCH2,ADC1_CH1
18	IO38	GPIO38,FSPIWP,SUBSPIWP
19	IO39	MTCK,GPIO39,CLK_OUT3,SUBSPICS1
20	IO17	RTC_GPIO17,GPIO17,U1TXD,ADC2_CH6
21	IO18	RTC_GPIO18,GPIO18,U1RXD,ADC2_CH7, CLK_OUT3
22	IO19	RTC_GPIO19,GPIO19,U1RTS,ADC2_CH8, CLK_OUT2,USB_D-
23	IO20	RTC_GPIO20,GPIO20,U1CTS,ADC2_CH9, CLK_OUT1,USB_D+

24	IO21	RTC_GPIO21,GPIO21
25	IO48	GPIO48,SPICLK_N_DIFF,SUBSPI_CLK_N_DIFF
27	IO33	GPIO33,FSPIHD,SUBSPIHD,SPIIO4
28	IO34	GPIO34,FSPICS0,SUBSPICS0,SPIIO5
29	IO35	GPIO35,FSPID,SUBSPID,SPIIO6
30	IO36	GPIO36,FSPICLK,SUBSPICLK,SPIIO7
31	IO37	GPIO37,FSPIQ,SUBSPIQ,SPIDQS
32	IO15	RTC_GPIO15,GPIO15,U0RTS,ADC2_CH4, XTAL_32K_P
33	IO16	RTC_GPIO16,GPIO16,U0CTS,ADC2_CH5, XTAL_32K_N
34	IO40	MTDO,GPIO40,CLK_OUT2
35	IO41	MTD1,GPIO41,CLK_OUT1
36	IO42	MTMS,GPIO42,
37	U0TX	U0TXD,GPIO43,CLK_OUT1
38	U0RX	U0RXD,GPIO44,CLK_OUT2
39	IO45	GPIO45
40	IO46	GPIO46
41	EN	High level: chip enable Low level: chip off Do not let the CHIP_PU pin float

Table 7 Module startup mode description

System boot mode			
Pin	**Default**	**SPI start-up model**	**Reboot download-Mode**
IO0	Pull-Up	1	0
IO46	pull-down	/	0

Note: some pins have been pulled up internally, please refer to the schematic diagram.

5. Schematic

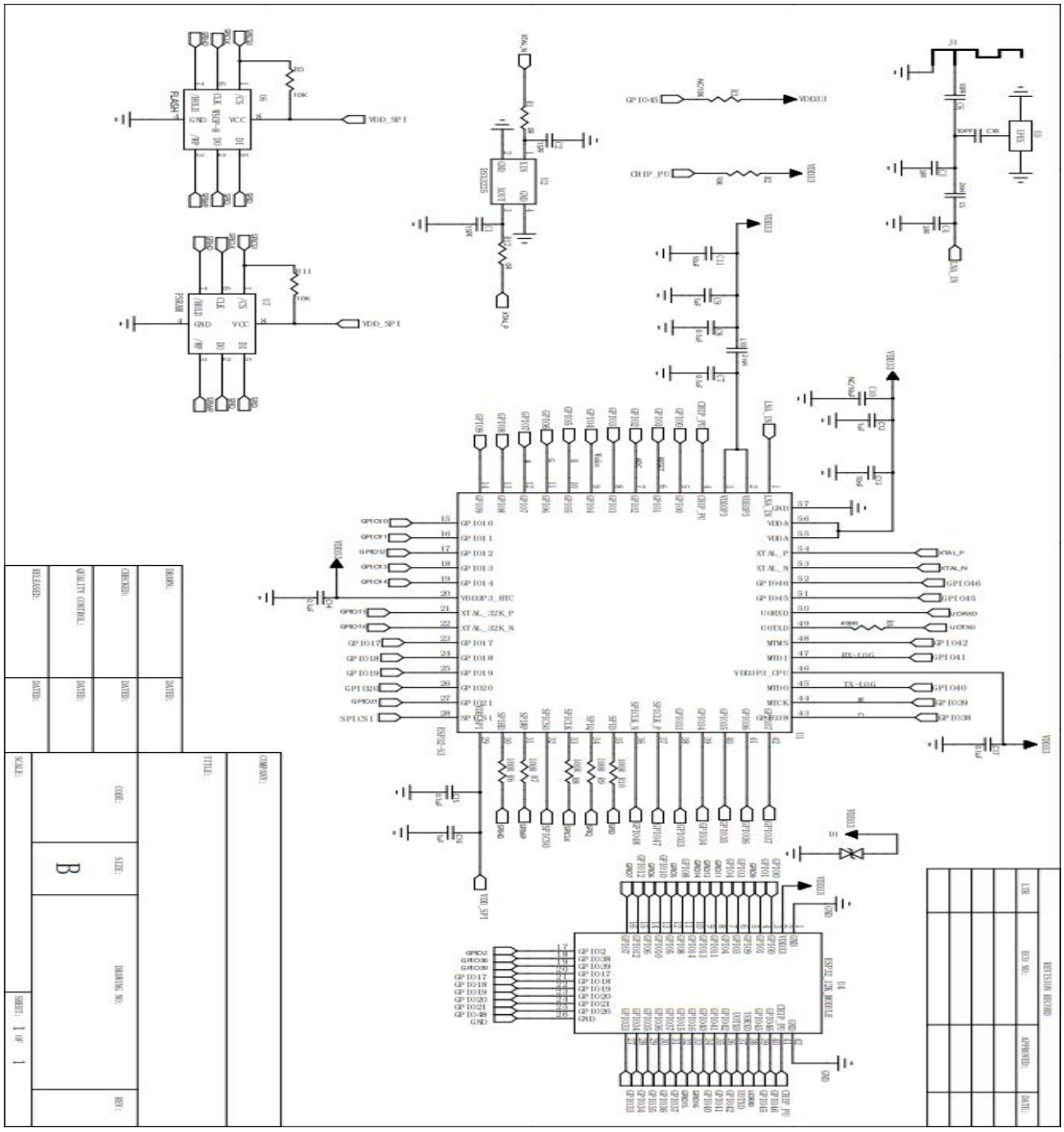


Figure 6 Module schematic

6. Antenna parameters

6.1. Test conditions for the antenna

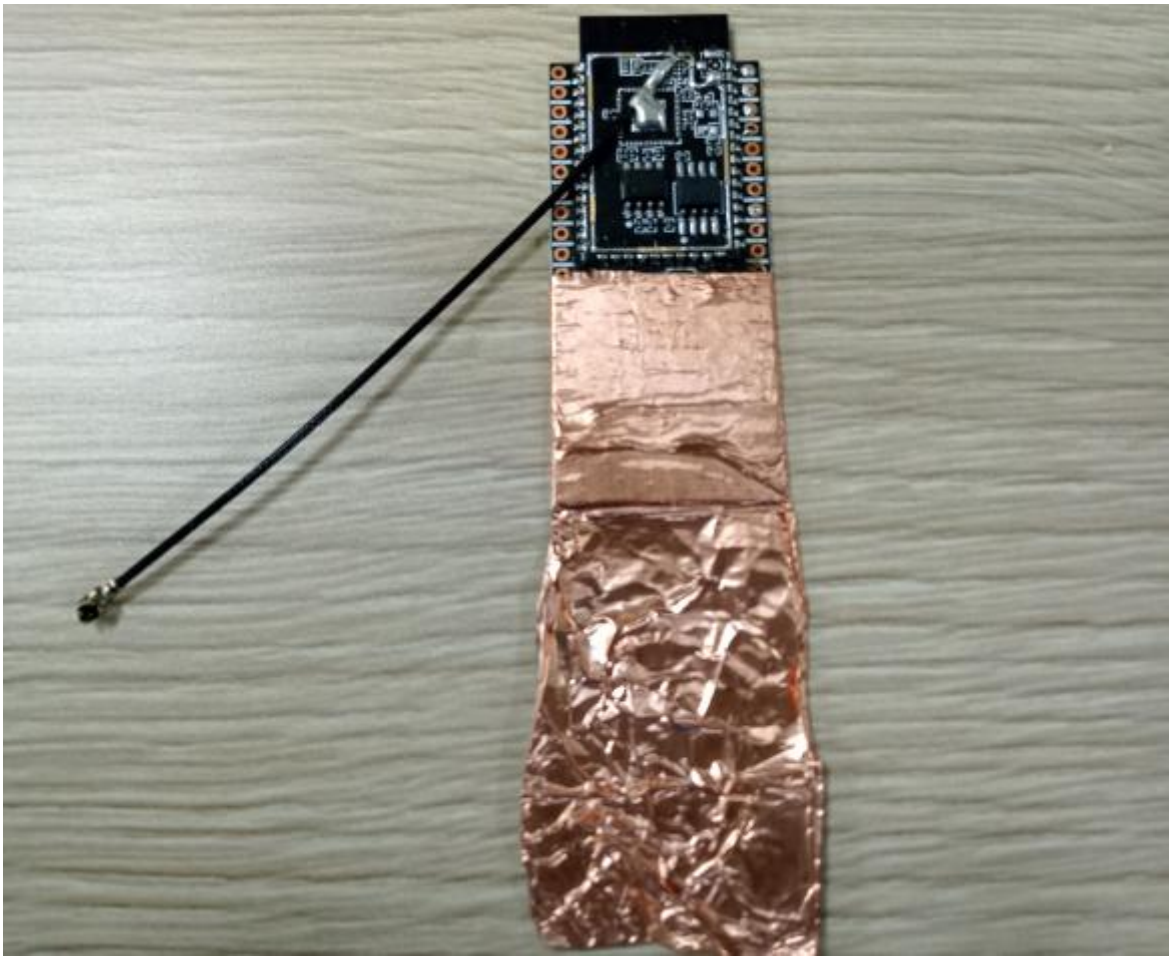


Figure 7 Simulates a scenario in which a user solders a module onto a motherboard

6.2. Antenna S parameter

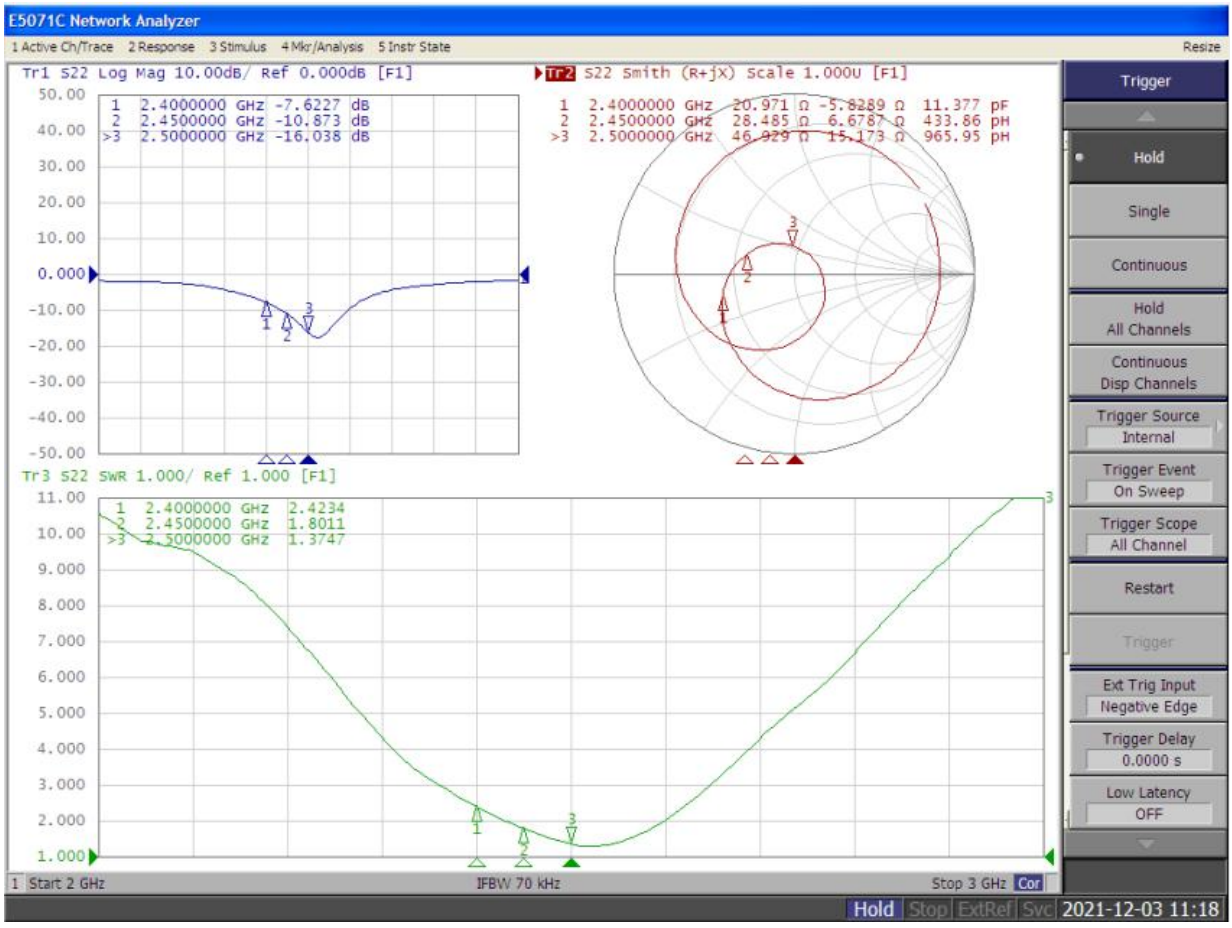


Figure 8 Antenna S parameters

6.3. Antenna Gain and Efficiency

Table 8 Antenna Gain and efficiency

Frequency ID	1	2	3	4	5	6	7	8	9	10	11
Frequency (MHz)	2400.0	2410.0	2420.0	2430.0	2440.0	2450.0	2460.0	2470.0	2480.0	2490.0	2500.0
Gain (dBi)	-1.84	-1.87	-1.94	-1.94	-1.92	-1.68	-1.52	-1.50	-1.58	-1.59	-1.74
Efficiency (%)	65.39	65.01	63.96	63.95	64.31	67.96	70.48	70.82	69.53	69.39	67.00

6.4. Antenna field type diagram

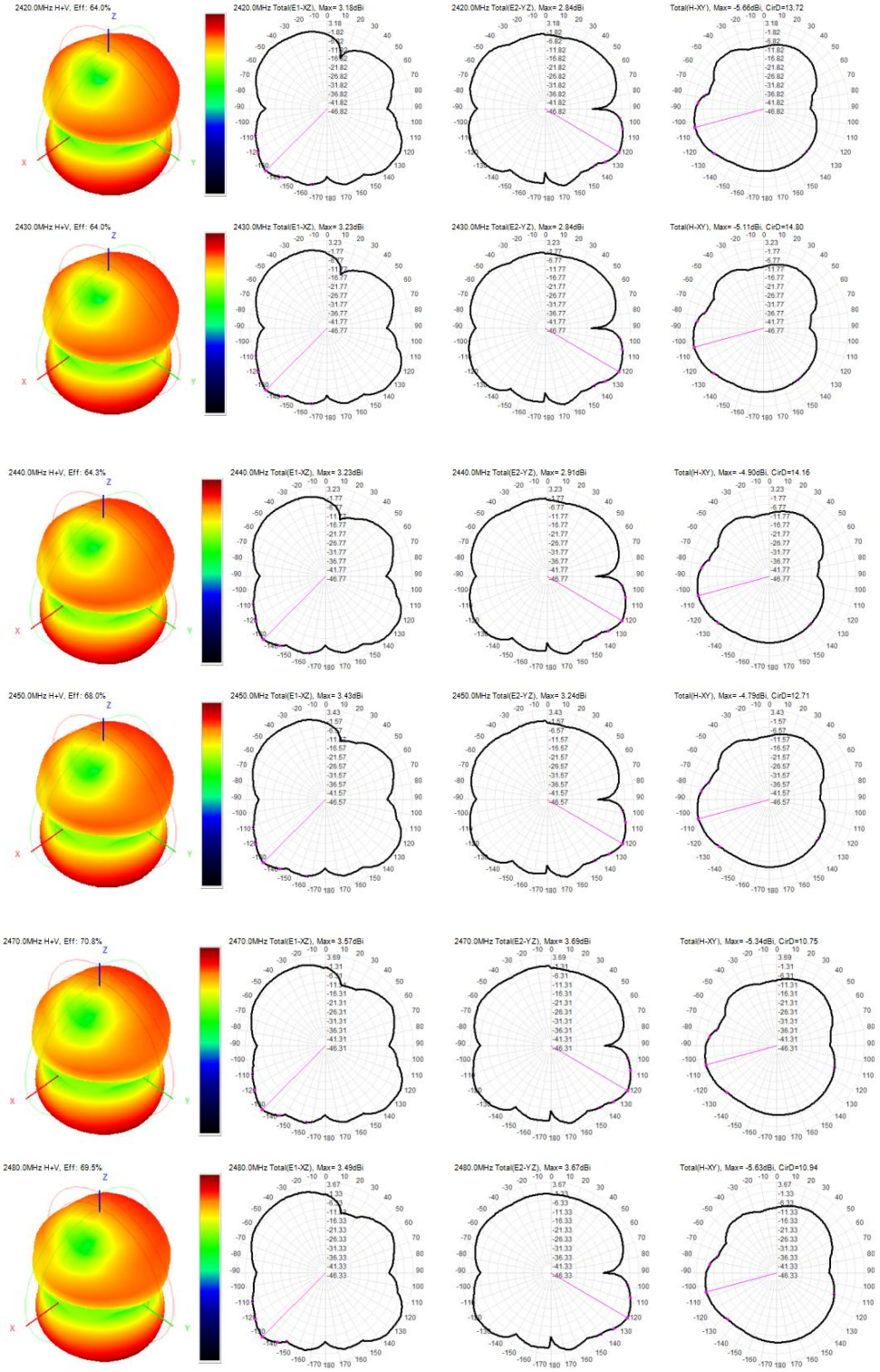


Figure 9 Antenna field type diagram

7. Design guidance

7.1. Module application circuit

(>= 500mA,suggest use DC-DC or LDO independent power supply)

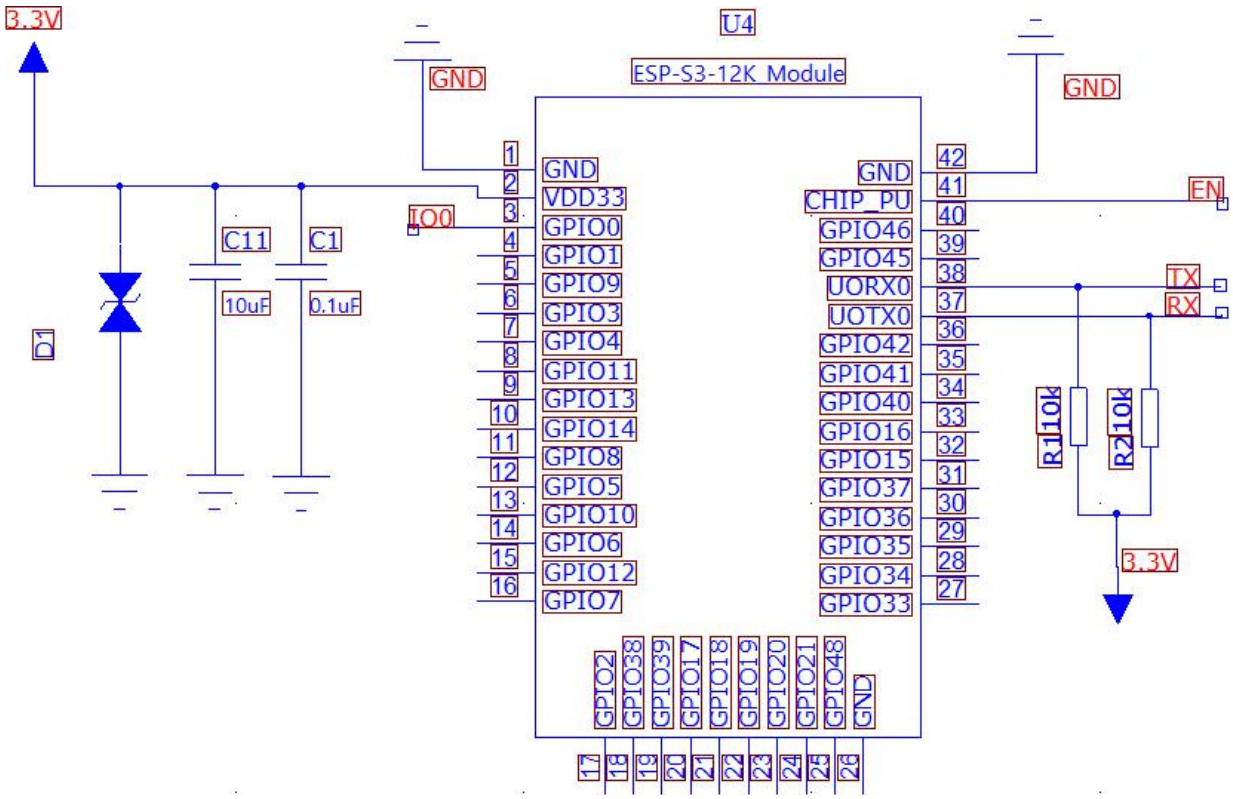


Figure 10 Application circuit diagram

Note：

- U0RX0 and U0TX0 require an external pull-up resistor, while U0RX0 is connected to TX of another machine and U0TX0 is connected to RX of another machine.
- IO0 is a start control pin, which is in normal working mode at high power and burning firmware mode at low power. Default high level inside the chip.

7.2. Antenna layout requirements

- The installation position on the motherboard suggests the following 2 ways:

Scheme 1:Put the module on the edge of the motherboard,And the antenna area extends out the edge of the motherboard.

Scheme 2:Put the module on the edge of the motherboard,and empty an area along the antenna position.

- To meet the performance of the on-board antenna,metal parts are not placed around the antenna,away from the high-frequency device

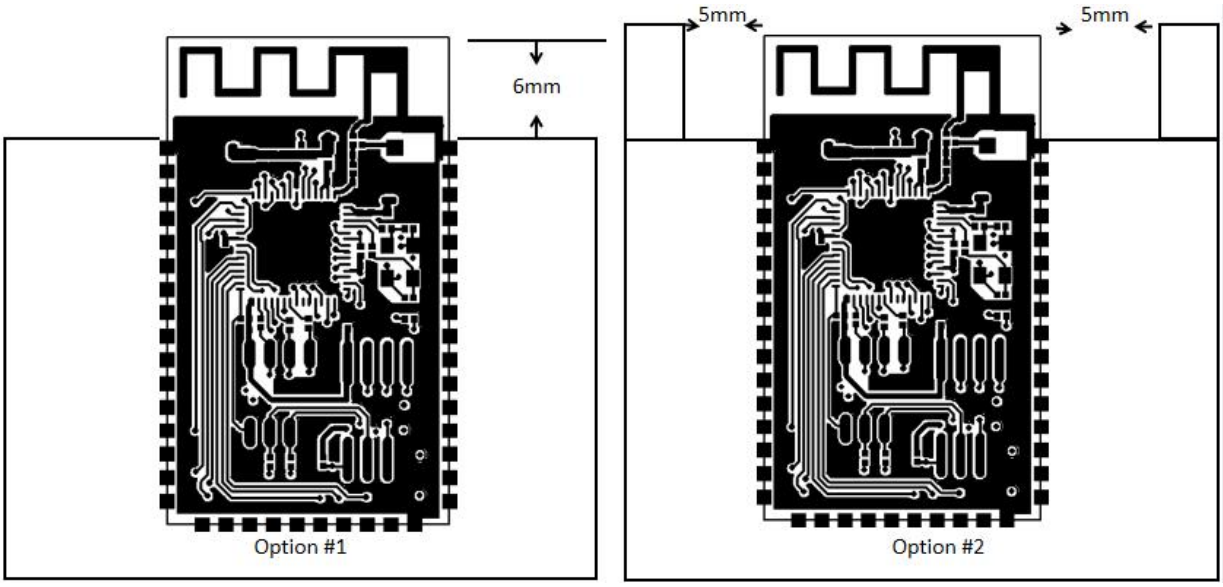


Figure 11 Schematic diagram of the antenna layout

7.3. Power supply

- Recommended 3.3V voltage,peak current over 200mA.
- Power supply is recommend to use LDO;If the DC-DC is used,the ripple is recommended to be controlled within 30mV
- DC-DC power supply circuit proposes to reserve the dynamic response capacitance to optimize the output ripple with large load changes.
- 3.3V power interface it is recommended to add ESD devices.

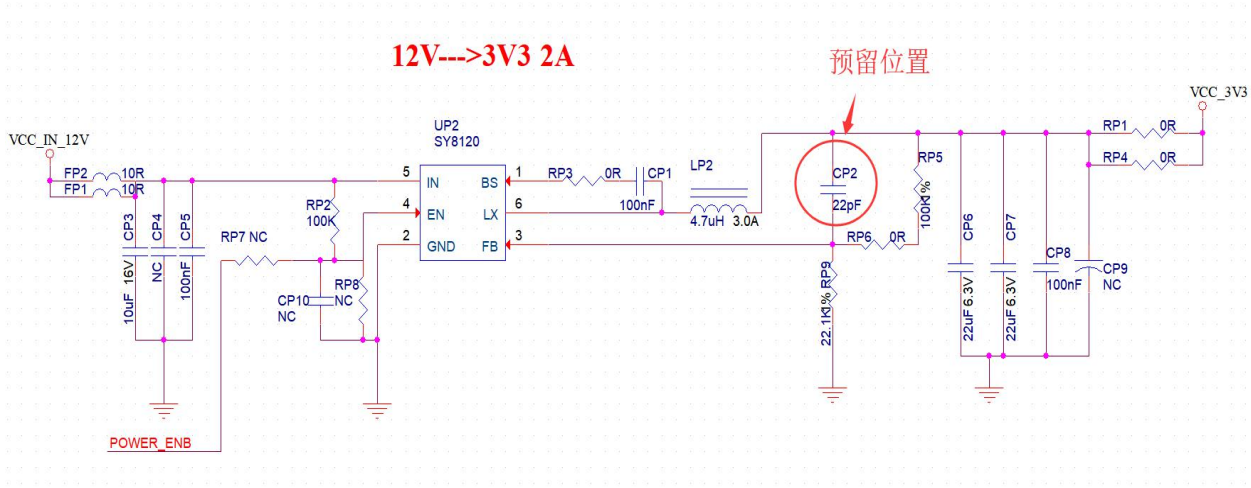


Figure 12 The DC-DC antihypertensive circuit diagram

7.4. GPIO

- Some IO ports are lead outside the module,if using,a proposed resistance of 10-100 ohms on the IO port.This suppresses the overshoot and enables smoother levels on both sides,helping for both EMI and ESD.
- The up and down of the special IO port should refer to the use instructions of the specification,which will affect the start-up configuration of the module.
- The IO port of the module is 3.3V,if the main control does not match the IO port level of the module,the level conversion circuit should be increased.
- If the IO port is directly connected to the peripheral interface,or terminals such as pin header,it is recommended to reserve ESD devices at the IO port line near the terminal.

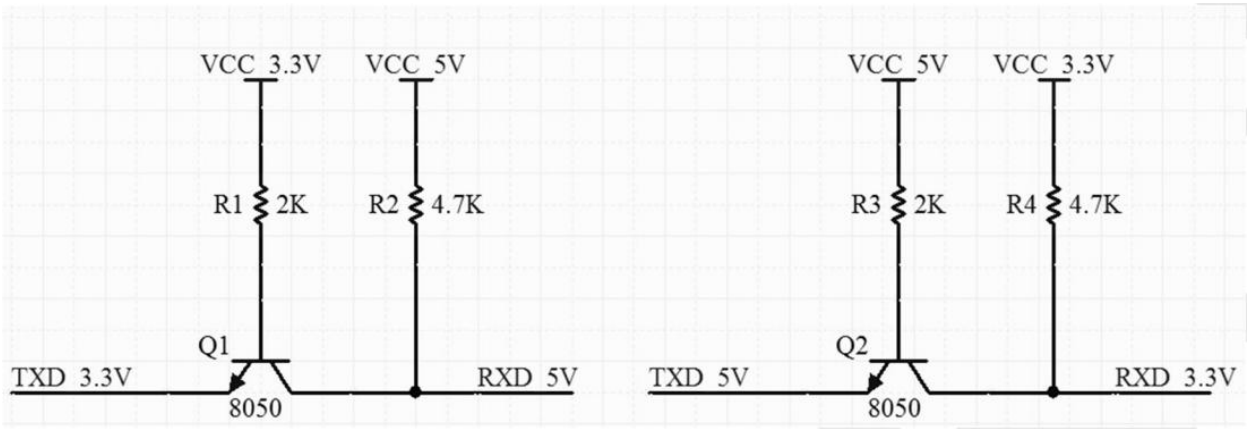


Figure 13 Level convert circuit

8. Flow welding curve diagram

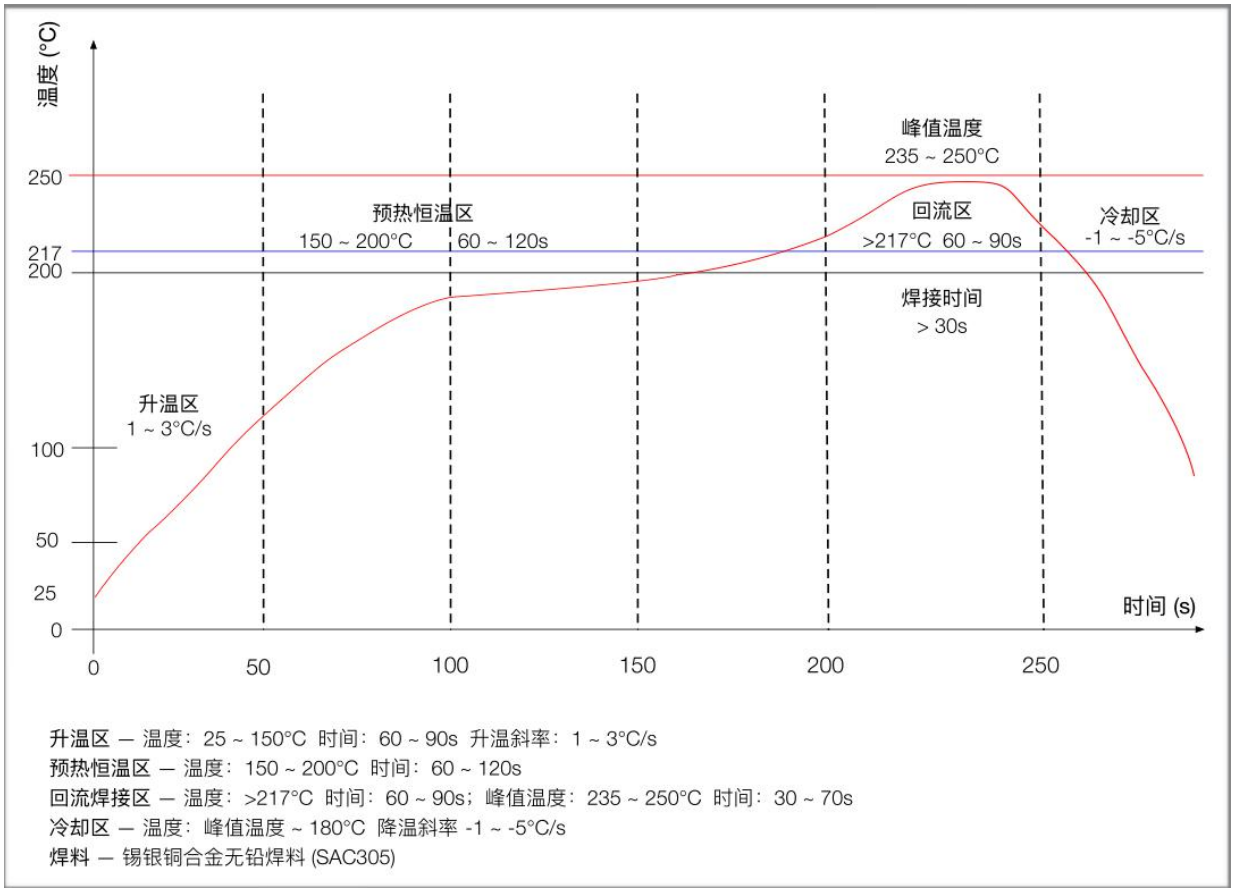


Figure 14 Flow welding diagram

9. Product related models

Table 9 Product related model list

Model	Power Supply	Package	Size	Antenna
ESP-S3-32S	3.0V ~ 3.6V，I>500mA	SMD-40	25.5*18.0*3.2(±0.2)mm	The on-board PCB antenna or external antenna connector is compatible
ESP-S3-12K	3.0V ~ 3.6V，I>500mA	SMD-42	31*18*3.2(±0.2) mm	The on-board PCB antenna or external antenna connector is compatible
NodeMCU-ESP-S3-32S	5V, I>500mA	DIP30	61*25.5*12.9(±0.2)mm	The on-board PCB antenna or external antenna connector is compatible
NodeMCU-ESP-S3-12K	5V, I>500mA	DIP42	58.5*25.5*12.9mm	The on-board PCB antenna or external antenna connector is compatible
Product related information https://docs.ai-thinker.com				

10. Product packaging information

ESP-S3-12K module was packaged in a tape,500pcs/reel.As shown in the below image:

Figure 15 Package and packing diagram